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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,239	06/25/2002	Mike Ryken	8782-US-PA	6389

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE  
7 FLOOR-1, NO. 100  
ROOSEVELT ROAD, SECTION 2  
TAIPEI, 100  
TAIWAN

EXAMINER

TSAI, HENRY

ART UNIT

PAPER NUMBER

2183

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/064,239

Applicant(s)

RYKEN, MIKE

Examiner

Henry W.H. Tsai

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 6/25/02.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s)     is/are withdrawn from consideration.
- 5) ☒ Claim(s) 13-16 is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☒ Claim(s) 8-12 is/are objected to.
- 8) ☐ Claim(s)     are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on     is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No.    .
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date    .
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date    .
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:    .

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**DETAILED ACTION**

***Claim Objections***

1. Claims 1-7 and 13-16 are objected to because of the following informalities:

in claim 1, line 5, "world" should read - word -; and

in claim 13, line 18, "the recirculated portion of the word length" lack proper antecedent basis. It is suggested to change "the recirculated portion of the word length" to - the portion of the word length fed back to the multiplexer -. Similar problems exist in claims 14 and 15.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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3. Claims 1-5, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Simar et al. (U.S. Patent No. 6,182,203) (hereafter referred to as Simar et al.'203).

Referring to claim 1, Simar et al.'203 discloses, as claimed, a method for fetching at least one word instruction from a memory in a word-based processor (see Figs. 9 and 24), wherein the word instruction includes types of a full-word instruction (such as the instruction A in Fig. 9 which is determined by the position in an instruction fetch packet, see also Fig. 24) or a half-word instruction (such as the instructions B-H in Fig. 9), the processor employs a data bus with a word length in bit, the method comprising: dividing the word length into a plurality of word units (such as the instructions A-H in Fig. 9, see also Fig. 24), wherein each of the word units has a size of  $2^n$  bits ( $32 = 2^5$  bits in instructions A-H in Fig. 9); checking a memory request to know whether or not the word instruction to be fetched is in a first type address or a second type address (by checking the position of the instruction in the instruction fetch packet, see Fig. 24), wherein the first type address is a sequential half-word non-aligned address (such as the instructions B-H in Fig. 9) and the second type address is other than the first type address (such as the instruction A in Fig. 9); fetching the word instruction

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at each of fetch cycles, if the second type address is a current status (since the instruction A is the first instruction in an instruction fetch packet); fetching the sequential half-word instruction simultaneously in the full word length at a first fetch cycle (since the instructions B-H are also fetched when the instruction fetch packet is fetched see Fig. 9, see also col. 14, line 34-35, regarding the instruction are always fetched eight at a time"), if the word instruction is at the first type address, wherein the half-word instructions are stored in the word units (the units having 32 bits each, see Fig. 9); and executing the half-word instructions without directly fetching the half-word instructions from the memory (since the instructions B-H have already been fetched) in next fetch cycles to the first fetch cycle.

As to claim 2, Simar et al.'203 also discloses: the second type address comprises a word aligned address (such as the instruction A in Fig. 9) and a non-sequential address (such as the instruction in the other packet see Fig. 9).

As to claim 3, Simar et al.'203 also discloses: the non-sequential address is an address not following a previous address by one word unit (such as the instruction in the other packet see Fig. 9).

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As to claim 4, Simar et al.'203 also discloses: the sequential half-word non-aligned address is an address following a previous address by one word unit (such as the instructions B-H sequentially following the previous address by one word unit, 32 bits, see Fig. 9).

As to claim 5, Simar et al.'203 also discloses: the size of the word unit is 8 bits, 16 bits or 32 bits (32 bits see Fig. 9).

As to claim 7, Simar et al.'203 also discloses: the step of executing the half-word instructions (such as the instructions B-H in Fig. 9) comprises obtaining instruction addresses (in the fetch stage, see Fig. 24) with respect to the half-word instructions and getting contents (in the dispatch stage, see Fig. 24) of the half-word instructions.

#### **Claim Rejections - 35 USC § 103**

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

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such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Simar et al.'203 in view of Pechanck et al. (U.S. Patent No. 6,321,322) (hereafter referred to as Pechanck et al.'322).

Simar et al.'203 discloses the claimed invention except for comprising: the full word instruction has a size of 64 bits and the half-word instruction has a size of 32 bits (in claim 6).

Pechanck et al.'322 discloses a system comprising instruction set formats having the full word instruction (instruction 16E see Fig. 1B) with a size of 64 bits and the half-word instruction (instruction type-2-A,B,C (12B) inside instruction 16C, see Fig. 1B) with a size of 32 bits.

Simar et al.'203's system is designed to use 32-bit instruction. However, 64-bit architectures have dominated the field of high-performance computing (see Col. 6, lines 25-26 in Pechanck et al.'322).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Simar et al.'203's system to comprise the full word instruction has a

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size of 64 bits and the half-word instruction has a size of 32 bits, as taught by Pechanck et al.'322, in order to increase the flexibility by also being able to use 64-bit instruction; and to improve the performance for the Simar et al.'203's system.

***Allowable Subject Matter***

6. Claims 8-12 are allowed.

7. Claim 13-16 would be allowable if rewritten or amended to overcome the rejection(s) under Claim Objections set forth in this Office action.

8. The following is a statement of reasons for the indication of allowable subject matter: Simar et al. (U.S. Patent No. 6,182,203) and Pechanck et al. (U.S. Patent No. 6,321,322), the closest references, and the other prior art do not teach or fairly suggest: the circuit in combination of a multiplexer; a flip-flop unit; and an OR logic gate for providing the recirculated portion of the word length and feeding back the recirculated portion of the word length to the multiplexer (in claim 8, and claim 13 recites the corresponding limitations).



### *Conclusion*

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bhandal et al.'602 discloses: a data processor with flexible multiply unit. The invention includes a pair of parallel 16X16 multipliers each with two 32-bit inputs and one 32-bit output. There are options to allow input half word and byte selection for four independent 8X8 or two independent 16 X 16 multiplications, real and imaginary parts of complex multiplication, pairs of partial sums for 32 X 32 multiplication, and partial sums for 16 X 32 multiplication. Shang et al.'980 discloses apparatus and method for parallel decoding of variable-length instructions in a superscalar pipelined data processing system. Using the indicators as delimiters of the sequence of to-be-decoded instructions, one or more non-overlapping subsequences of the sequence of data words are identified, wherein each subsequence of data words is comprised in a different, sequential to-be-decoded instruction.

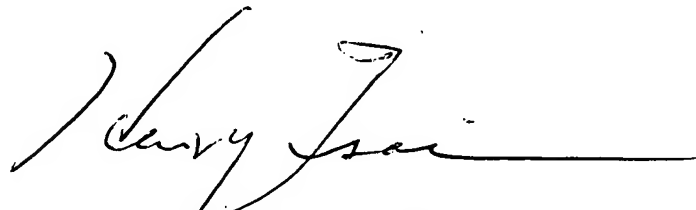
### *Contact Information*

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry

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Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC central telephone number, 571-272-2100.

11. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into the Group at fax number: 703-872-9306. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

  
HENRY W. H. TSAI  
PRIMARY EXAMINER

December 2, 2004